100

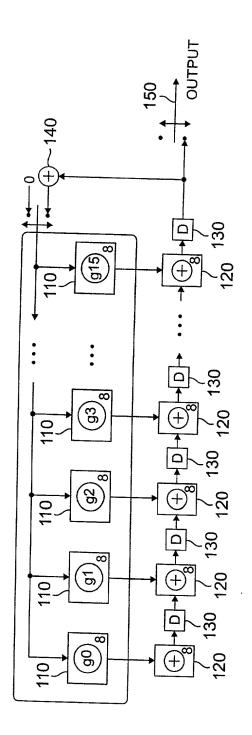


FIG. 1 (PRIOR ART)

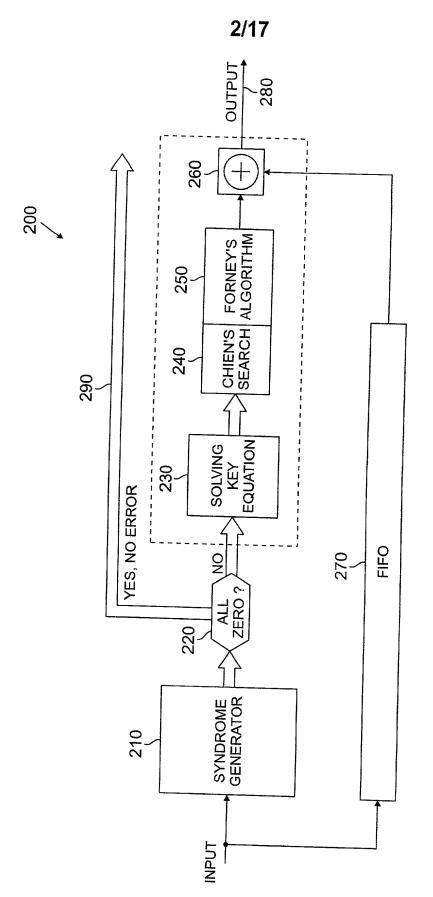
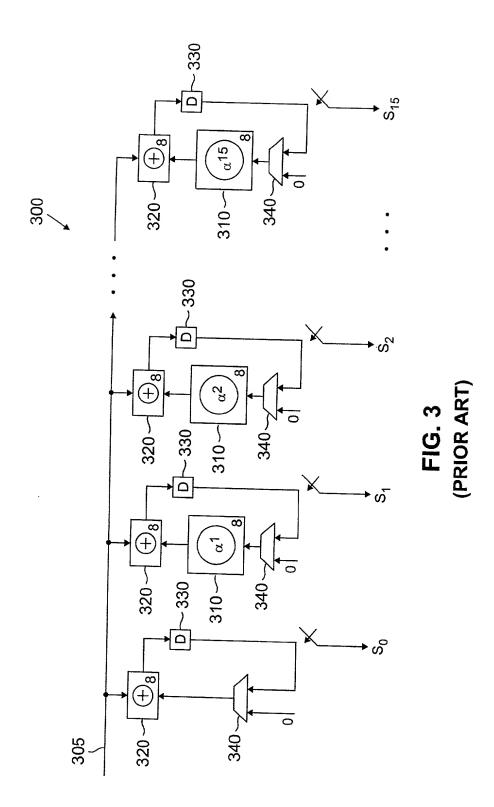


FIG. 2 (PRIOR ART)



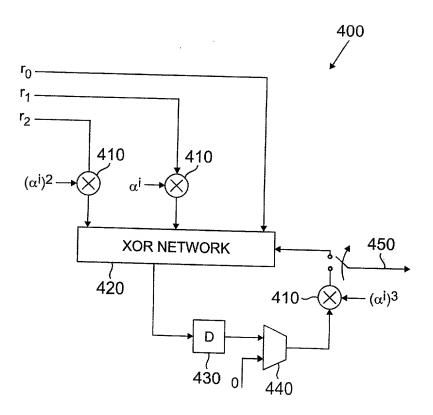
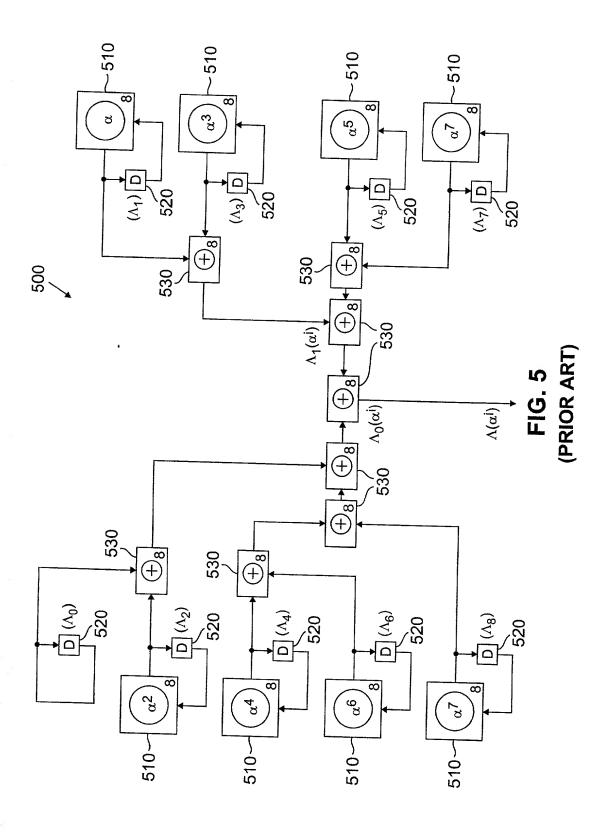
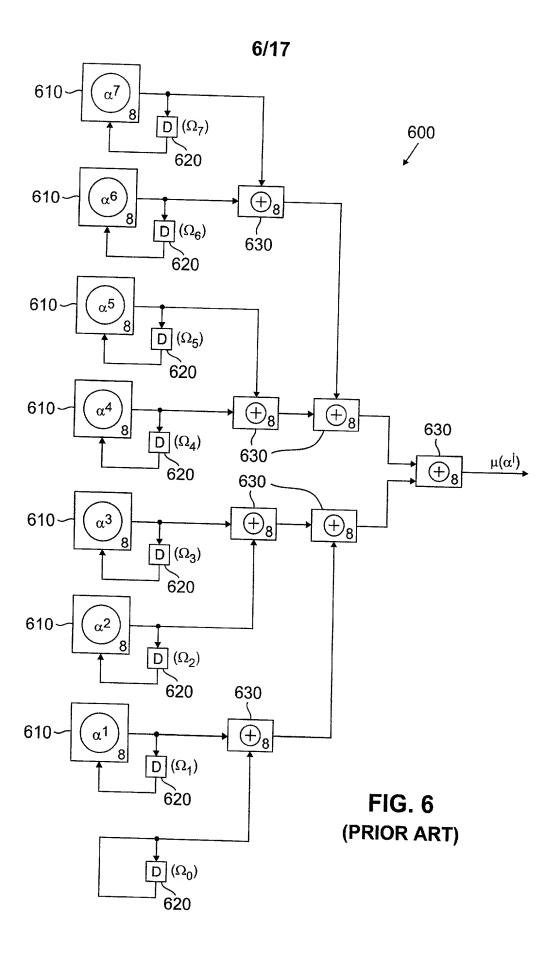
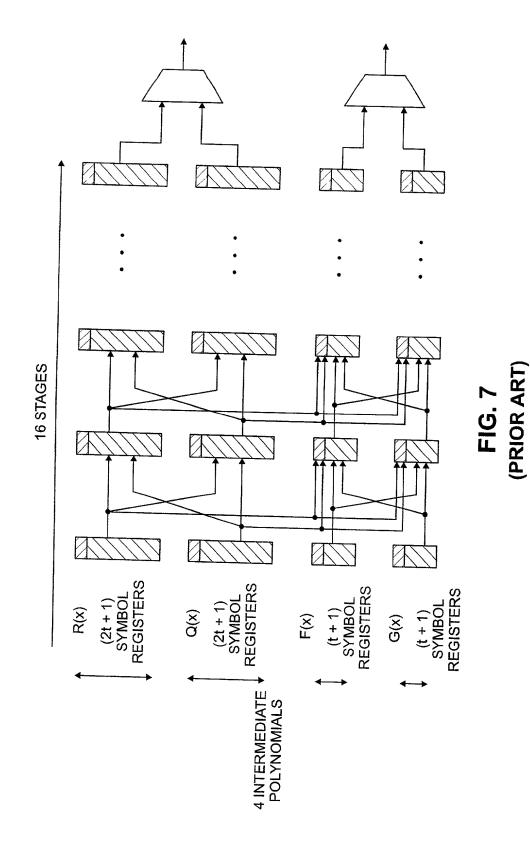
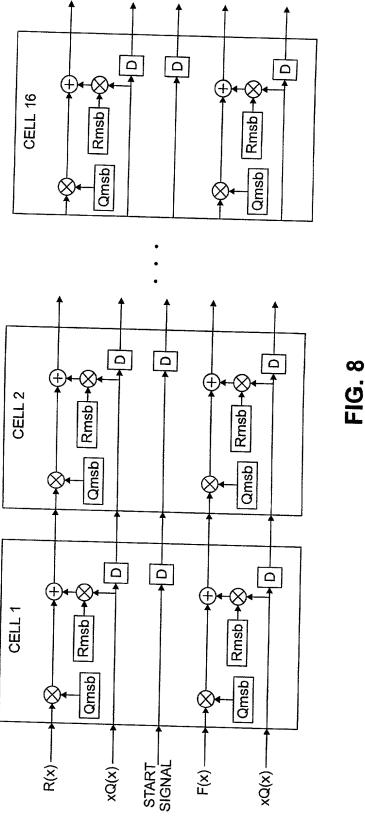


FIG. 4









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FIG. 8 (PRIOR ART)

The state of the s

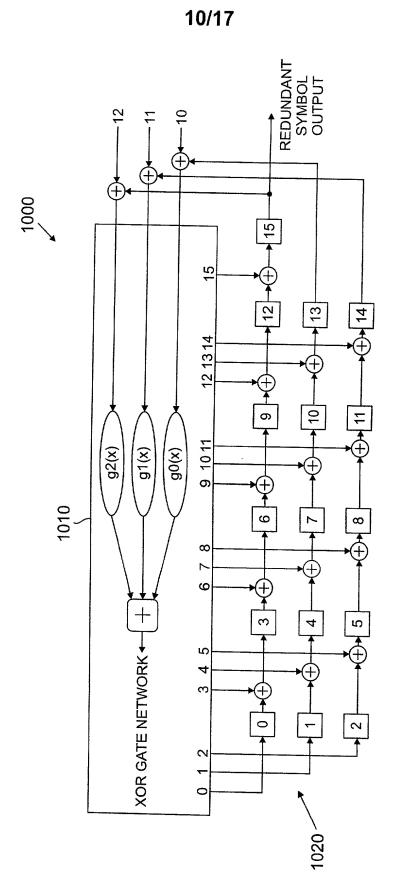


FIG. 10(a)

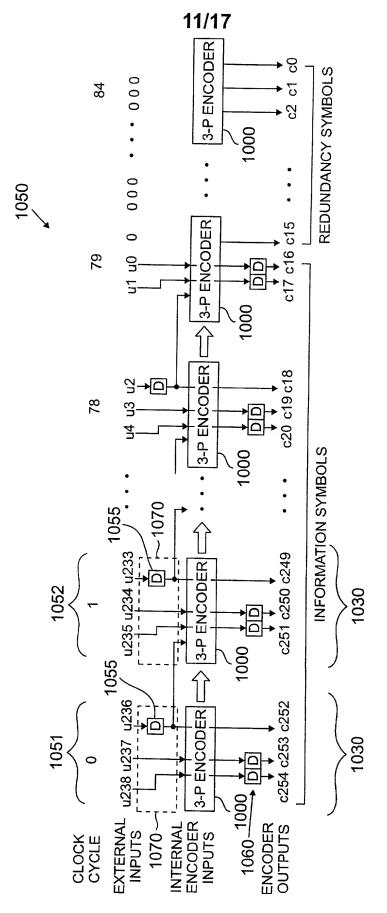


FIG. 10(b)

the state of the s

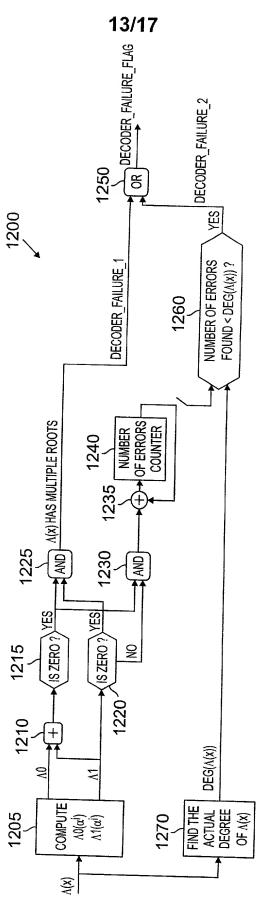


FIG. 12

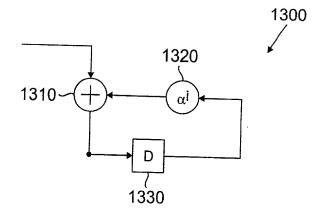


FIG. 13(a)

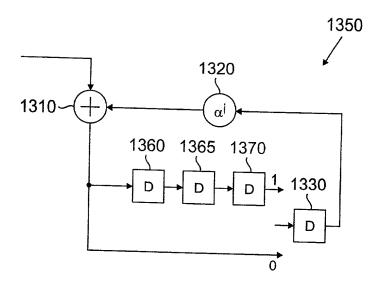


FIG. 13(b)

1400

16 BYTES PER CYCLE @ 83 MHz

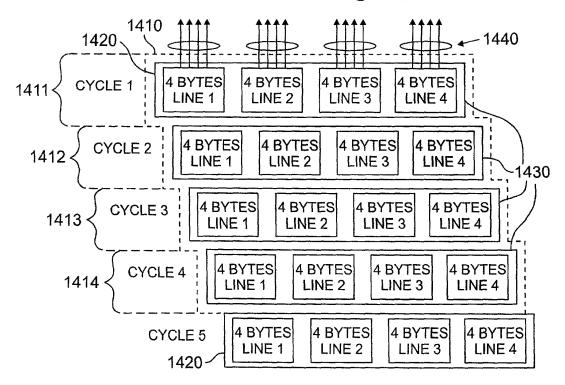


FIG. 14

1500

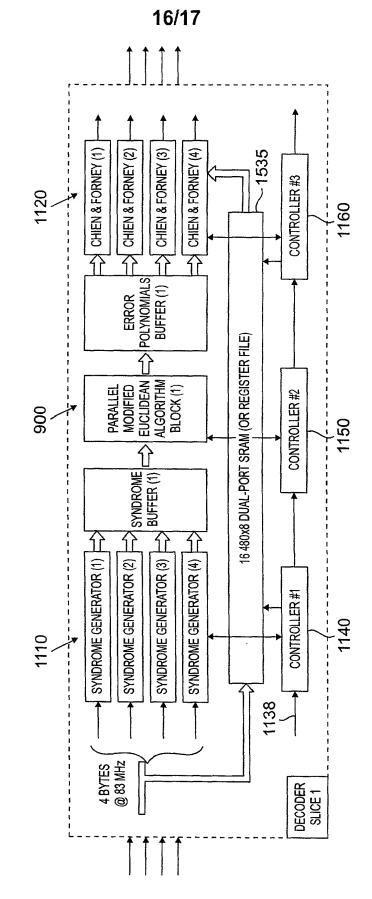


FIG. 1:

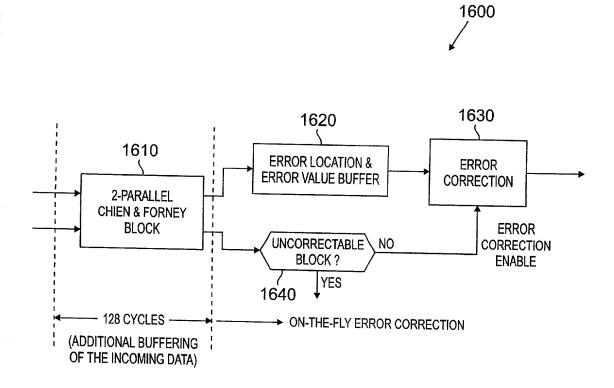


FIG. 16